CLAIMS

What is claimed is:

1. A circuit board apparatus comprising:

a semiconductor package defined by a substrate having a matrix of conductive contact pads on both the top and bottom surfaces of the substrate; and

two interposers for receiving said semiconductor package, the interposer defined by a body having a matrix of interposer contact bumps on both the inner and outer surfaces of the body, each interposer contact bump comprising an electrically conductive path and shaped to abut a contact pad of said semiconductor package and contact pads of said PCB.

2. The apparatus of claim 1 wherein the contact pads of the semiconductor package are uniformly spaced.

3. The apparatus of claim 1 wherein the semiconductor package is a land grid array package.

4. The apparatus of claim 1 wherein the contact pads of the interposer are uniformly spaced.

5. The apparatus of claim 1 wherein the contact pads on the top surface of the semiconductor package support debugging and test operations.

6. The apparatus of claim 5 wherein the contact pads on the bottom surface of the semiconductor package are designated for production operations.

7. The apparatus of claim 1 wherein the number of interposer contact pads on the inner surface of the interposer exceeds the number of contact pads on the top surface of the semiconductor package.

8. The apparatus of claim 1 wherein the interposer contact pads on the inner surface of the interposer are arranged in the same pattern, pitch and spacing as the contact pads on the top surface of the semiconductor package.

9. The apparatus of claim 8 wherein the semiconductor contact pads have a 1.27 mm pitch or smaller.

10. The apparatus of claim 1 wherein the substrate supports 1443 signals to be collected.

11. A circuit board apparatus comprising:

a semiconductor package defined by a substrate having a matrix of conductive contact pads on both the top and bottom surfaces of the substrate;

an interposer for receiving said semiconductor package, the interposer defined by a body having a matrix of interposer contact pads on both the inner and outer surfaces of the body, each interposer contact pad comprising a metal coating and shaped to abut a contact pad of said semiconductor package;

a heat sink for absorbing or dissipating any excess heat generated by said semiconductor package; and

a gasket for providing sufficient force to the apparatus.

12. The apparatus of claim 11 wherein the gasket comprises a sponge.

13. The apparatus of claim 12 wherein the gasket comprises a silicon sponge.

14. The apparatus of claim 13 wherein the gasket comprises a Young's modulus in the range of 100 to 200 kpsi.

15. The apparatus of claim 14 wherein the gasket behaves elastically up to 50% compression.

16. The apparatus of claim 11 wherein the gasket has a width of 0.150 inches and a height of 0.125 to 0.1875 inches.

17. The apparatus of claim 16 wherein the gasket is compressed approximately 20 to 40% of its original height when the apparatus is fully assembled.

18. A processor comprising a substrate having a matrix of conductive contact pads on the bottom surface of the substrate and a test port on the top surface of the substrate.

19. The processor of claim 18 wherein the test port comprises a conductive contact pad.

20. The processor of claim 18 wherein the test port is designated for debugging and test operations.

21. The processor of claim 18 wherein the contact pads on the bottom surface of the processor are designated for production operations.

22. The processor of claim 18 wherein the test port on the top surface of the substrate possesses approximately the same contact density as the contact pads on the bottom surface of the substrate.

23. The processor of claim 18 wherein the test port on the top surface of the substrate possesses approximately the same signal integrity as the contact pads on the bottom surface of the substrate.

24. The processor of claim 18 wherein the test port on the top surface of the substrate possesses approximately the same reliability as the contact pads on the bottom surface of the substrate.